REMARKS

Claims 1-25 are pending in the present application. Claims 19-25 have been presented herewith.

Telephone Interview

Applicant's representative acknowledges the courtesy extended by the Examiner during the telephone interview conducted on April 13, 2007. Fig. 3A of the Tuda et al. reference (U.S. Patent No. 5,132,937) was discussed during the interview. No agreement was reached during the interview. The substance of the discussion is reflected in the following comments.

Claim Rejections-35 U.S.C. 103

Claims 1-18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Tuda et al. reference (U.S. Patent No. 5,132,937) in view of the Kono et al. reference (U.S. Patent No. 5,455,536). This rejection is respectfully traversed for the following reasons.

The circuit for detecting an abnormal operation of memory of claim 1 includes in combination a delay circuit "for delaying an output data output from the memory for a predetermined period of time and for outputting a delayed data responsive thereto"; and a comparison circuit "for outputting a noncoincidence signal when the output data output from the memory and the delayed data are not coincident with each other".

Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

Applicant respectfully submits that claims 1-18 would not have been obvious in view of the prior art as relied upon by the Examiner, for at least the reasons set forth in the Amendment dated August 3, 2006, and the Request for Reconsideration dated January 16, 2007. The Examiner has failed to clearly establish on the record how the Tuda et al. reference as specifically relied upon can be interpreted as including a delay circuit that delays an output data output from a memory. Particularly, column address signal Adc and row address signal Adr as input to address change detecting circuit 211, are not output from memory cell array 10, and are not delayed, as would be necessary to meet the features of the claims.

In view of the comments provided in the Advisory Action dated February 28, 2007, the Examiner has apparently somehow interpreted address change detecting circuit 211 and delay circuit 212 in Fig. 3A of the Tuda et al. reference together as the delay circuit of claim 1. However, delay circuit 212 in Fig. 3A of the Tuda et al. reference is described in column 4, lines 6-8 as delaying **an ATD pulse which is an output of address change detecting circuit 211.** Delay circuit 212 of the Tuda et al. reference is not described or even remotely suggested as delaying an output data output from memory cell array 10, as would be necessary to meet the features of claim 1.

On page 2 of the Advisory Action dated February 28, 2007, the Examiner has

asserted the following:

"Tuda explicitly demonstrated a connectivity from Adc + Adr (i.e., address and data input/output) from memory to a delay circuit 212 via change circuit 211. This is very obvious to an ordinary skill in the art to realize that Adc + Adr input/output come from the memory connect to delay circuit in ensuring the error thoroughly detected and corrected via the delayed and comparison processes".

Applicant respectfully submits that the above noted comments as offered by the Examiner in the Advisory Action dated February 28, 2007, clearly demonstrate that the Examiner has misinterpreted the Tuda et al. reference. The Examiner has apparently interpreted Adc + Adr in Figs. 3A of the Tuda et al. reference as address and data input/output from memory. However, the Tuda et al. reference does not disclose or even remotely suggest that signals Adc + Adr are data input/output from memory.

Particularly, in column 3, lines 49-56 of the Tuda et al. reference, Adc is specifically described as an **externally applied** column address signal, and Adr is specifically described as an **externally applied** row address signal. Column address decoder 11 thus **receives externally applied** column address signal Adc to select a corresponding column of respective sub arrays in memory cell array 10. Similarly, row address decoder 12 **receives externally applied** row address signal Adr to select a corresponding row of respective sub arrays in memory cell array 10. One of basic entry level engineering skill would readily understand from this above noted description in column 3 of the Tuda et al. reference that column address signal Adc and row address

signal Adr are not output from memory cell array 10, or decoders 11 and 12, as believed by the Examiner.

In the telephone interview conducted on April 13, 2007, the Examiner asserted that the brackets denoted Adc and Adr respectively adjacent column address decoder 11 and row address decoder 12 in Fig. 3A of the Tuda et al. reference indicate that address signals Adc and Adr are respectively output from memory cell array 10 via column address decoder 11 and row address decoder 12. This interpretation offered by the Examiner is clearly erroneous. As previously noted, decoders 11 and 12 respectively receive address signals Adc and Adr, and subsequently decode these signals, so as to provide access to memory cell array 10. Address signals Adc and Adr are **externally applied**. It is fairly evident that the Examiner in this case lacks basic understanding of the semiconductor memory circuit and function disclosed in the Tuda et al. reference.

Applicant respectfully submits that the Tuda et al. reference therefore does not disclose or make obvious the features of claim 1. Applicant therefore respectfully submits that the circuit for detecting an abnormal operation of memory of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1-7 is improper for at least these reasons.

With further regard to this rejection, the Examiner has secondarily relied upon the Kono et al. reference as apparently disclosing a comparison circuit "for outputting a

not-coincident signal from carrying out a comparison between the data and the delayed data". That is, the Examiner has apparently interpreted delay 22 in Fig. 3 of the Kono et al. reference as equivalent to the delay circuit of claim 1.

However, as described beginning in column 4, line 21 of the Kono et al. reference with respect to Fig. 3, a received IF signal is input to demodulator 12, which executes coherent demodulation of the received IF signal and thus outputs received data S_0. Delay 22 delays input received data S_0 and provides the corresponding delayed signal to comparator 24 as S_2, whereby comparator 24 performs comparison between corrected data S_1 and delayed data S_2 at a timing controlled by clock CL. **Delay 22 in Fig. 3 of the Kono et al. reference does not delay an output data output from a memory.** This should be particularly clear because the Kono et al. reference is concerned with demodulation, not with detecting abnormal operation of a memory. Particularly, there is no memory coupled to delay 22 in Fig. 3 of the Kono et al. reference.

Moreover, comparator 24 in Fig. 3 of the Kono et al. reference compares a delayed version of the received demodulated signal with an error corrected version of the received demodulated signal. Comparator 24 does not compare a signal output from a memory with a delayed version of the signal output from the memory. That is, the circuit in Fig. 3 of the Kono et al. reference compares an error corrected version of a signal with a delayed version of the signal, and does not compare a signal with a delayed version of a signal, as would be necessary to meet the features of claim 1.

Moreover, one of ordinary skill would have no motivation to modify the semiconductor memory device of the Tuda et al. reference in view of the demodulator of the Kono et al. reference, because the teachings are clearly from divergent, unrelated fields. As such, the Kono et al. reference does not overcome the above noted deficiencies of the primarily relied upon Tuda et al. reference. Applicant therefore respectfully submits that the circuit for detecting an abnormal operation of memory of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1-7 is improper for at least the above reasons.

With further regard to this rejection, since the Tuda et al. and Kono et al. references do not disclose a delay circuit for delaying an output data output from memory, the prior art as relied upon by the Examiner clearly does not disclose or even remotely suggest a comparison circuit that compares output data output from a memory with output data from a memory that is delayed, to provide a non-coincidence signal as would be necessary to meet the further features of claim 1. Applicant therefore respectfully submits that the circuit for detecting an abnormal operation of memory of claim 1 would not have been obvious over the prior art as relied upon by the Examiner, taken singularly or together, and that this rejection of claims 1-7 is improper for at least these additional reasons.

With regard to claim 2, the Examiner has very generally asserted that column 4, lines 45 through to column 5, line 25 and Fig. 6 of the Tuda et al. reference **explicitly**

teach that an access speed of a memory is detected. However, as asserted in the Amendment dated August 3, 2006, the above noted portions of the Tuda et al. reference as relied upon do not specifically or explicitly describe, mention, or consider access speed of a memory, or more particularly detection thereof. In contrast, a result storing mode is described in column 5 of the Tuda et al. reference. Applicant therefore respectfully submits that claim 2 would not have been obvious in view of the prior art as relied upon, and that this rejection of claim 2 is improper for at least these additional reasons.

Regarding claim 3, since the Tuda et al. reference as relied upon by the Examiner does not disclose a comparison circuit that outputs a non-coincidence signal based on comparison of output data from a memory with output data from a memory that is delayed, the Tuda et al. reference clearly does not explicitly or otherwise teach a circuit that holds address information in the case of non-coincidence in response to a non-coincidence signal, as asserted by the Examiner.

Regarding claim 6, column 4, lines 2-41 and column 5, lines 67 through to column 6, lines 3 of the Tuda et al. reference do not explicitly or otherwise teach that delay circuit 212 in Fig. 3A has a delay time that can be adjusted, as would be necessary to meet the features of claim 6.

These above noted arguments with respect to claims 2, 3 and 6 have been presented in the previous Amendment dated August 3, 2006. The Examiner has however failed to address these arguments in the Final Office Action dated October 16,

2006. **The Examiner is respectfully requested to take note of all the above noted traversals, and to clearly answer the substance of the traversals, so that the record will be clear in the event this application proceeds to Appeal.**

The integrated circuit of claim 8 includes in combination a memory; a delay circuit "which delays an output data from the memory and outputs a delayed data responsive thereto"; and a comparison circuit "which compares the output data from the memory and the delayed data, and which outputs a noncoincidence signal when the output data and the delayed data are not coincident".

As asserted above with respect to claim 1, the delay circuit 212 in Fig. 3A of the Tuda et al. reference delays an ATD pulse output from address change detecting circuit 211, **not data output from a memory**, as would be necessary to meet the features of claim 8. Moreover, address change detecting circuit 211 has input thereto column address signal Adc and row address signal Adr, and therefore does not compare output data from a memory with output data from a memory that is delayed, as would be necessary to meet the further features of claim 8. The Kono et al. reference as relied upon does not overcome these deficiencies. Applicant therefore respectfully submits that claim 8 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 8, 17 and 18 is improper for at for at least these reasons.

With further regard to this rejection, the Tuda et al. reference does not appear to include first and second latch circuits as featured in claim 17. With regard to claim 18,

the Tuda et al. reference does not provide a noncoincidence signal as featured, and thus does not include an address information storing circuit which stores address information when a noncoincidence signal is output by a comparison circuit.

Applicant also respectfully submits that the method for detecting an abnormal operation of memory of claim 9 would not have been obvious in view of the relied upon prior art for at least somewhat similar reasons as set forth above with respect to claim 1. Particularly, delay circuit 212 in Fig. 3A of the Tuda et al. reference does not delay an output data output from a memory. Also, address change detecting circuit 211 in Fig. 3A of the Tuda et al. reference does not output a noncoincidence signal based on comparison of output data output from a memory with output data from a memory that is delayed. The Kono et al. reference as relied upon does not overcome these deficiencies. Applicant therefore respectfully submits that the method for detecting an abnormal operation of memory of claim 9 would not have been obvious in view of the prior art as relied upon taken singularly or together, and that this rejection of claims 9-16 is improper for at for at least these reasons.

With further regard to this rejection, Applicant respectfully submits that the Tuda et al. reference as specifically relied upon does not detect access speed of memory as featured in claim 10, and does not hold address information in case of noncoincidence in response to a noncoincidence signal as featured in claim 11. Moreover, since delay circuit 212 in Fig. 3A of the Tuda et al. reference is not described as having adjustable delay time, the Tuda et al. reference does not disclose the features of claim 15. The

Kono et al. reference as relied upon does not overcome these deficiencies. Applicant therefore respectfully submits that claims 10, 11 and 15 would not have been obvious for at least these additional reasons.

Claims 19-25

The integrated circuit of claim 19 includes in combination a memory "that stores data"; a delay circuit "directly coupled to the memory, that delays stored data output from the memory for a predetermined period of time and that outputs delayed data responsive thereto"; and a comparison circuit "coupled to the memory and the delay circuit, that compares the stored data output from the memory with the delayed data, and that outputs a noncoincidence signal when the stored data output from the memory and the delayed data are not coincident with each other, the noncoincident signal indicative of abnormal operation of the memory".

Applicant respectfully submits that the integrated circuit of claim 19 distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above. Particularly, address change detecting circuit 211 and delay circuit 212 in Fig. 3A of the Tuda et al. reference cannot collectively be interpreted as the delay circuit of claim 19, because address change detecting circuit 211 in particular is not directly coupled to memory cell array 10. Delay circuit 212 in Fig. 3A of the Tuda et al. reference delays an ATD pulse output from address change detecting circuit 211, not stored data output from a

memory.

Conclusion

The Examiner is respectfully requested to take note of an answer each of the traversals set forth above, including those pertaining to dependent claims, so that the record with respect to this application may be complete.

The Examiner is further respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

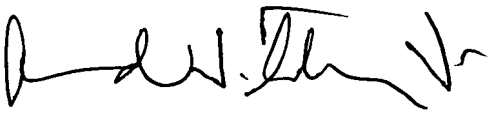
Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of three (3) months to April 16, 2007, for the period in which to file a response to the outstanding Office Action. The required fee of $1020.00 should be charged to Deposit Account No. 50-0238.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740